Confirmation No. 5709

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MATTHEWS, *et al.*	Examiner:	Daley, C.
Serial No.:	10/814,426	Group Art Unit:	2111
Filed:	March 31, 2004	Docket No.:	81339624US01 (5797-00500)
Title:	COMMUNICATION APPARATUS IMPLEMENTING TIME DOMAIN ISOLATION WITH RESTRICTED BUS ACCESS		

BRIEF ON APPEAL

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed April 29, 2008 and in response to the rejections of claims 1-56 as set forth in the Final Office Action dated January 9, 2008 and in acknowledgment of the Advisory Action dated March 17, 2008.

Please charge Deposit Account number 50-0996 (NXPS.251PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 018021/0819 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-56 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

All amendments have been entered.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued

by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 21, an example embodiment of the present invention is directed to a method of operating a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) including a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7), the method comprising: arbitrating between requests to access a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27) by a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) and one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:24); receiving a signal indicative of a change in a mode of operation of the RF circuit (*see, e.g.*, page 12:16-22); and restricting access requests issued by the one or more other bus masters to access the bus in response to the signal (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 26, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) transceiver (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF transceiver, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF transceiver (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 32, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) front-end circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF front-end circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27) and one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit (*see, e.g.*, page 12:16-22); and wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip (*see, e.g.*, integrated circuit die 140 shown in Fig. 1, and page 6:26-27).

Commensurate with independent claim 38, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a

signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 42, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters according to an arbitration policy during at least a portion of a duration of an inactive mode of operation of the RF circuit; wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit (*see, e.g.*, page 12:16-22 and page 19:12-23).

Commensurate with independent claim 49, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) transceiver (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF transceiver, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented

during a first period of operation; wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 53, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation; wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation beginning a predetermined amount of time prior to an active mode of the RF circuit (*see, e.g.*, page 12:16-22).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The remaining ground of rejection is listed below.

A. Claims 1-56 stand rejected under 35 U.S.C. § 103(a) over Shaeffer (U.S. Patent No. 6,963,626) in view of Hadwiger (U.S. Patent No. 6,738,845).

VII. Argument

Appellant requests that the Board reverse the rejections of all pending claims 1-56 because the cited combination does not correspond to the claimed invention, and because the Examiner fails to provide sufficient detail regarding the proposed combination of the Shaeffer and Hadwiger references to enable Appellant to determine the propriety of the asserted combination.

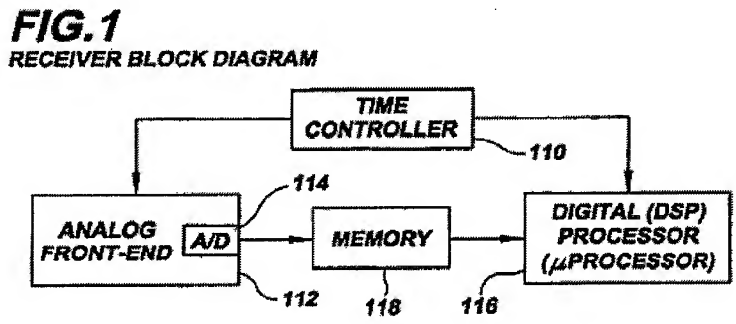
A. The rejection of claims 1-41 and 49-56 under U.S.C. § 103(a) over Shaeffer and Hadwiger should be reversed because the proposed combination fails to correspond to the claimed invention.

A purported obviousness rejection based on a combination of references fails unless the references teach or suggest all the recited claim elements. In this instance, the cited combination does not correspond to the claimed invention which includes, for example, aspects directed to restricting access requests issued by one or more other bus masters in response to a signal indicative of a change in a mode of operation of an RF circuit. With particular regard to claims 1-41 and 49-56, the Examiner's argument in the Final Office Action of January 9, 2008 (hereafter "the Examiner's response"), does not address restricting issued (*e.g.,* by a bus master) access requests as in the claimed invention. Aspects of Appellant's claimed invention allow for a bus master to continue operating while, for example, running a transition interrupt procedure (*see, e.g.*, Appellant's Specification at paragraphs 35-41). In some implementations, other bus masters continue to operate and therefore may issue access requests; the AHB bus is capable of restricting those access requests. Thus, there is a clear (and often important) differentiation between restricting an "*issued* access request" and shutting down a bus master so that no requests issue. Claims 1-41 and 49-56 each include aspects directed to restricting *issued* access requests. This is in contrast to the Examiner's asserted combination, which would restrict accesses only to the extent that requests are prevented from ever issuing.

Appellant submits that the lack of correspondence between the claimed invention and the asserted combination is best understood by a detailed explanation of the Examiner's proposed combination of the Shaeffer and Hadwiger references. Appellant notes that while the Examiner has identified the various elements of the references, little,

if any, explanation has been provided regarding how these elements are to be combined as is required by, for example, 35 U.S.C § 132. Appellant has assumed that the asserted combination attempts to create a hypothetical combination as described below. Appellant presented this hypothetical combination in the Response dated February 20, 2008, and the record is clear that Examiner has neither refuted Appellant's hypothetical combination nor provided any explanation regarding any other possible combination of the cited references.

The Examiner's combination relies upon elements present in both of the block diagrams shown in Figures 1 and 2 of Shaeffer. As discussed in Shaeffer and relied upon in the rejection, the DSP 116 can be powered down when the analog front-end 114 is active (*see, e.g.*, Shaeffer at Col. 5, lines 47-62). Shaeffer's Figure 1 is reproduced below for the convenience of the Board.



Shaeffer's Figure 1.

The Examiner's combination further relies upon elements present in the block diagram of Figure 2 of the Hadwiger reference. As discussed in Hadwiger and relied upon in the rejection, the bus arbitration module (BAM) 211 arbitrates between the DSP system 201 and various devices (*see, e.g.*, Hadwgier at Col. 4, lines 31-55). Hadwiger's Figure 2 is reproduced below for the convenience of the Board:

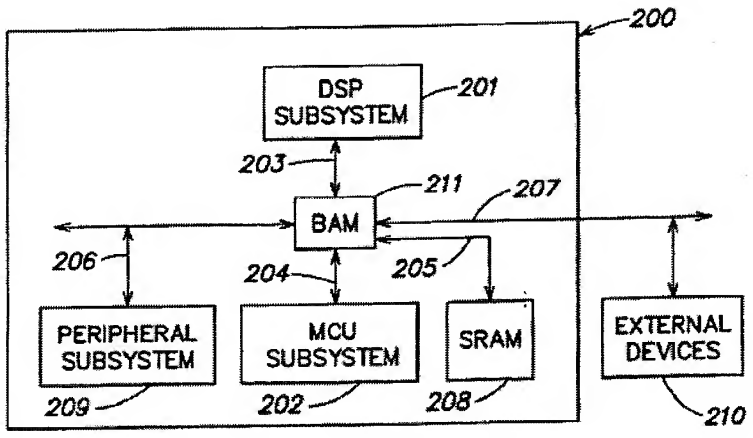


FIG. 2

Hadwiger's Figure 2.

As best as can be determined, the Examiner's combination proposes adding the BAM and peripherals of Hadwiger's Figure 2 to DSP 116 of Shaeffer's Figure 1 (*e.g.*, DSP 116 essentially replaces DSP subsystem 201). This results in a system similar to the combined Figures 1 and 2 shown below:

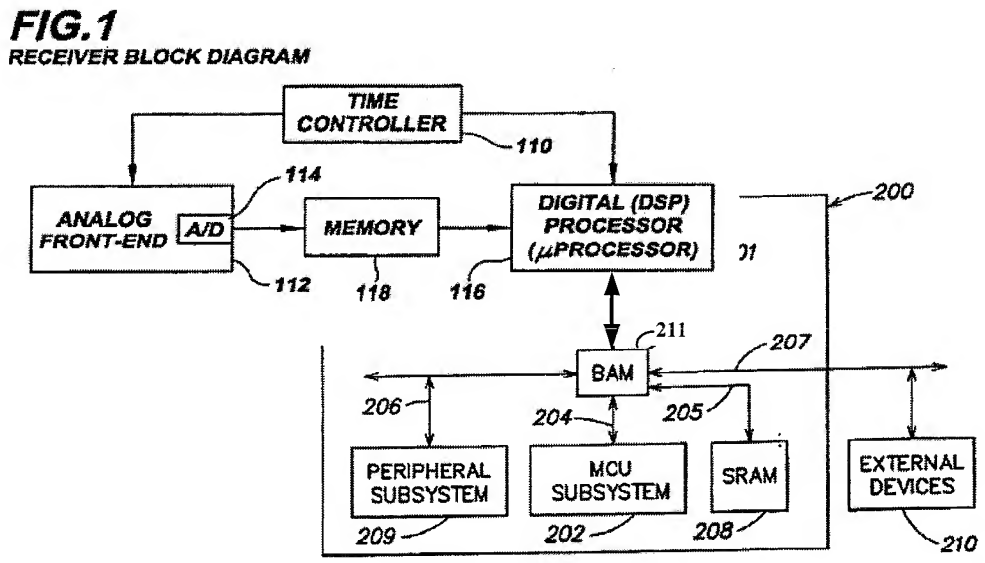


FIG. 2

It should be apparent that

1) when deactivated by time controller 110, DSP 116 would not issue any requests, and

2) arbitration decisions of BAM 211 are not responsive to time controller 110.

The following discussion explains why the aforementioned elements are relevant to the lack of correspondence between the asserted combination and the claimed invention.

Appellant respectfully submits that the Examiner's definition of restriction, which states that in the prior art "no access requests would be generated, and thus, there would be no access requests to restrict," does not address Appellant's previous arguments (*see also*, Appellant's Responses dated February 20, 2008 and July 25, 2007, both of which are incorporated by reference in their entirely). Thus, the Examiner has explicitly stated that the combination restricts access requests by preventing issuance/generation thereof (*i.e.,* no access requests are issued); however, various claim limitations are directed to restricting *issued* (past tense) requests. Thus, the claim limitations are directed to restriction of a request that has been issued. Correspondence to such limitations cannot be shown by simply preventing an access request from issuing because the limitations require that the access request actually issues. In the Advisory Action, the Examiner states that Appellant's "specification provides no limiting definition for restricting, therefore the examiner is may interpret broadly the meaning of said term." Once again the Examiner continues to focus on the meaning of the word "restricting" instead of on what the claim limitations require to be restricted (*i.e.,* issued access requests). As such, the Examiner's asserted combination does not correspond to the claimed invention because no access requests are issued and thus the asserted combination does not restrict issued requests. Accordingly, the cited combination does not correspond to the claimed invention.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-41 and 49-56 fails, and therefore must be reversed.

B. The rejection of claims 42-48 under U.S.C. § 103(a) over Shaeffer and Hadwiger should be reversed because the proposed combination fails to correspond to the claimed invention.

The cited combination further fails to correspond to aspects of the claimed invention directed to the bus arbiter implementing a less favorable arbitration policy for the one or more other bus masters in response to a signal indicated a change to an active mode of operation. With particular regard to claims 42-48, Appellant submits that the Examiner's response fails to show correspondence to a bus arbiter that implements a less favorable arbitration policy. Neither reference alone nor in combination teaches or suggests a bus arbiter that implements a less favorable arbitration policy. Instead, the Shaeffer reference teaches powering down the processor, while the Hadwiger reference teaches a bus arbiter. As the Examiner's response merely identifies elements of the Shaeffer and Hadwiger references (*i.e.*, a shut down signal and an arbiter), there is no support in the record for a modification to the arbiter of Hadwiger. Instead, as asserted by the Examiner's response, the combination prevents issuance of access requests using the power down function of the Shaeffer reference, whereas the arbiter of the Hadwiger reference would not restrict access requests because the Examiner has explicitly stated that they are never issued/generated. Put another way, Hadwiger appears to teach that the arbiter maintains the same arbitration policy and the Shaeffer reference does not teach or suggest modifying an arbiter. Thus, regardless of whether the processor is powered down as taught by Shaeffer, the arbiter maintains the same arbitration policy. As the arbiter of Hadwiger neither 1) responds to any signal indicating a change to an active mode, nor 2) implements a less favorable arbitration policy, the cited combination fails to correspond to the claimed invention.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 42-48 fails, and therefore must be reversed.

C. The rejection of claims 1-56 under U.S.C. § 103(a) over Shaeffer and Hadwiger should be reversed because the Examiner fails to provide sufficient detail regarding the proposed combination.

The Examiner has provided insufficient detail to enable Appellant to determine the propriety of the asserted combination. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Appellant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.")

In this instance Appellant has reviewed the cited portions of the references and submits that these portions do not provide clarification regarding how the skilled artisan would combine the references or how such a combination would function. For example, it is unclear whether the Examiner is proposing to replace Shaeffer's DSP 116 with Hadwiger's DSP 201, MCU 22 and BAM 211, or whether these elements of Hadwiger would be added in addition to Shaeffer's DSP 116. In another example, it is unclear how the above mentioned elements of Hadwiger would function responsive to Shaeffer's time controller 110. In an effort to facilitate prosecution and develop a clear issue, Appellant has proposed the hypothetical combination that is discussed above. The Examiner, however, has not provided any clarification regarding the proposed combination.

Moreover, the Examiner's lack of specificity is further exacerbated by contradictory statements regarding the alleged teachings of the cited references. For example, the Examiner states that Shaeffer both has and does not have one or more other bus masters. Specifically, the Examiner asserts that Shaeffer teaches restricting accesses by the one or more other bus masters in response to a signal indicative of a change in a mode of operation of the RF circuit. *See, e.g.,* page 2 of the Examiner's response. The Examiner also states that Shaeffer does not disclose one or more other bus masters coupled to the bus. *See, e.g.,* page 3 of the Examiner's response. Appellant submits that it is illogical to assert that Shaeffer teaches restricting accesses by the one or more other bus masters when the reference does not even have one or more other bus masters.

In view of the above, Appellant maintains that it is not possible to be certain, with any particularity, what the Examiner's asserted combination includes and/or how any such combination would function. Without clarification of how the asserted combination would function (and support for such functionality in prior art) the Examiner has done little more than identify elements of the prior art.

There are many reasons why the Examiner is required to particularly identify and analyze an assertion combination. For example, to establish a *prima facie* case of obviousness the Examiner must provide a reason to combine the elements. Appellant respectfully submits that the specifics of how the asserted elements would function together are necessary to 1) judge whether the combination (not just the individual elements) in fact corresponds to the claimed invention and 2) determine whether a proper reason to combine the elements exists. As the record, including the cited references and the Examiner's response, is deficient regarding support for such details, Appellant submits the rejections are improper and cannot stand.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-56 fails, and therefore must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-56 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/814,426)

1. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;
wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit.

2. The communication apparatus as recited in Claim 1 wherein the signal is indicative of a change to an active mode of operation of the RF circuit.

3. The communication apparatus as recited in Claim 2 wherein the signal indicates a change to a transmission mode of operation of the RF circuit.

4. The communication apparatus as recited in Claim 2 wherein the signal indicates a change to a reception mode of operation of the RF circuit.

5. The communication apparatus as recited in Claim 2 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

6. The communication apparatus as recited in Claim 1 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

7. The communication apparatus as recited in Claim 1 wherein the signal indicative of a change of mode of operation of the RF circuit is generated by a timing circuit.

8. The communication apparatus as recited in Claim 1 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

9. The communication apparatus as recited in Claim 1 wherein the first bus master is a microcontroller unit (MCU).

10. The communication apparatus as recited in Claim 1 wherein the first bus master is a digital signal processor (DSP).

11. The communication apparatus as recited in Claim 9 wherein an interrupt signal is provided to the MCU and wherein an interrupt service routine executed by the MCU in response to assertion of the interrupt signal is performed when accesses by masters other than the first bus master to the bus are restricted.

12. The communication apparatus as recited in Claim 11 wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit.

13. The communication apparatus as recited in Claim 1 wherein the bus is a multi-layer bus, wherein the first bus master is provided exclusive access to one layer of the bus in response to assertion of the signal while the one or more other bus masters are allowed access to another layer of the multi-layer bus.

14. The communication apparatus as recited in Claim 6 wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit.

15. The communication apparatus as recited in Claim 6 wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit.

16. The communication apparatus as recited in Claim 1 wherein the bus arbiter is configured to restrict the granting of ownership of the bus to the one or more other bus masters in response to the signal.

17. The communication apparatus as recited in Claim 1 wherein the one or more other bus masters are configured to inhibit requests to gain ownership of the bus in response to the signal.

18. The communication apparatus as recited in Claim 1 wherein accesses by the one or more other bus masters are restricted by implementing a less favorable arbitration policy for the one or more other bus masters in response to the signal.

19. The communication apparatus as recited in Claim 1 wherein accesses by the one or more other bus masters to the bus are restricted by terminating burst transfers early in response to the signal.

20. The communication apparatus as recited in Claim 1 wherein the signal indicative of a change of mode of operation of the RF circuit is generated in response to execution of a software instruction.

21. A method of operating a communication apparatus including a radio frequency (RF) circuit and a digital processing circuit, the method comprising:

arbitrating between requests to access a bus by a first bus master and one or more other bus masters;

receiving a signal indicative of a change in a mode of operation of the RF circuit; and

restricting access requests issued by the one or more other bus masters to access the bus in response to the signal.

22. The method as recited in Claim 21 wherein accesses by the one or more bus masters are restricted by implementing a less favorable arbitration policy for the one or more bus masters in response to the signal.

23. The method as recited in Claim 21 wherein the signal is indicative of a change to an active mode of operation of the RF circuit.

24. The method as recited in Claim 23 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

25. The method as recited in Claim 25 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

26. A mobile phone comprising:

a radio frequency (RF) transceiver for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF transceiver, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;

wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF transceiver.

27. The mobile phone as recited in Claim 26 wherein the signal is indicative of a change to an active mode of operation of the RF transceiver.

28. The mobile phone as recited in Claim 27 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF transceiver.

29. The mobile phone as recited in Claim 26 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

30. The mobile phone as recited in Claim 26 wherein the signal indicative of a change of mode of operation of the RF transceiver is generated by a timing circuit.

31. The mobile phone as recited in Claim 26 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

32. A mobile phone comprising:

a radio frequency (RF) front-end circuit for operating on a radio frequency signal;

a digital processing circuit coupled to the RF front-end circuit, wherein the digital processing circuit includes a first bus master coupled to a bus and one or more other bus masters coupled to the bus; and

a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;

wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit; and

wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip.

33. The mobile phone as recited in Claim 32 wherein the signal is indicative of a change to an active mode of operation of the RF front-end circuit.

34. The mobile phone as recited in Claim 33 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF front-end circuit.

35. The mobile phone as recited in Claim 32 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

36. The mobile phone as recited in Claim 32 wherein the signal indicative of a change of mode of operation of the RF front-end circuit is generated by a timing circuit.

37. The mobile phone as recited in Claim 32 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

38. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;
wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

39. The communication apparatus as recited in Claim 38 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

40. The communication apparatus as recited in Claim 38 wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit.

41. The communication apparatus as recited in Claim 38 wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit.

42. A communication apparatus comprising:

a radio frequency (RF) circuit for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters according to an arbitration policy during at least a portion of a duration of an inactive mode of operation of the RF circuit;

wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit.

43. The communication apparatus as recited in Claim 42 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

44. The communication apparatus as recited in Claim 42 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

45. The communication apparatus as recited in Claim 42 wherein the first bus master is a microcontroller unit (MCU).

46. The communication apparatus as recited in Claim 45 wherein an interrupt service routine executed by the MCU in response to assertion of an interrupt signal is performed when the bus arbiter implements the less favorable arbitration policy for the one or more other bus masters

47. The communication apparatus as recited in Claim 46 wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit.

48. The communication apparatus as recited in Claim 42 wherein the RF circuit and the digital processing circuit are integrated on a single chip.

49. A mobile phone comprising:

a radio frequency (RF) transceiver for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF transceiver, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation;

wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

50. The mobile phone as recited in Claim 49 wherein the first bus master is provided exclusive access to the bus during the second period of operation.

51. The mobile phone as recited in Claim 49 wherein the shutdown mode includes disabling at least a portion of the digital processing circuit.

52. The mobile phone as recited in Claim 49 wherein the shutdown mode includes disabling a clock that clocks at least a portion of the digital processing circuit.

53. A communication apparatus comprising:

a radio frequency (RF) circuit for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation;

wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation beginning a predetermined amount of time prior to an active mode of the RF circuit.

54. The communication apparatus as recited in Claim 53 wherein the first bus master is provided exclusive access to the bus during the second period of operation.

55. The communication apparatus as recited in Claim 53 wherein the second period of operation is controlled by a timing circuit.

56. The communication apparatus as recited in Claim 53 wherein the bus arbiter is configured to implement a less favorable arbitration policy for the one or more other bus masters during the second period of operation.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.